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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/846,671	04/30/97	KO	K 11675.114

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IM22/0830

EXAMINER	
GOUDREAU, G	
ART UNIT	**PAPER NUMBER**
1763	11

DATE MAILED: 08/30/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

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U.S. G.P.O. 2000 ; 465-188/25266

Office Action Summary

Application No.	Applicant(s)
08-846,671	Ko
Examiner	**Group Art Unit**
George Goudreau	1763

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (MONTH(S)) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on (3-13-00' to 5-30-00')(i.e., paper #7-10).

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-46, 50-54 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) 1-10, 12 is/are allowed.

☒ Claim(s) 11, 13-22, 24-38, 40-46, 50-54 is/are rejected.

☒ Claim(s) 23, 39 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 7

☒ Notice of References Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

15. This action will not be made final due to the new grounds of rejection.

16. Claims 11, 13-17, 19-21, 27, 29-36, 43-46, and 51-53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

-In claims 13, 29, 31, 43-44, and 51, the plasma density should be recited as ions/cm3 instead of the way in which applicant claims the plasma density.;

-Claim 11 is redundant upon claim 1 upon which it depends.; and

-Claim 19, and 21 claim the same subject matter as each other, and therefore are redundant. (It is unclear to the examiner what the intended difference in scope between these two claims is. These claims are vague, and indefinite in this regard.)

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai (5,821,594).

Kasai discloses a process for forming a multi-layer semiconductor structure which is comprised of the following steps:

-A pad oxide layer (33) is formed onto the surface of source/drain regions (33) of a cz-Si wafer.;

-A conductive gate (27) is formed on the surface of the pad oxide layer (33). The conductive gate has a Si3N4 cap (28) on top of it. The conductive gate also has 2 different Si3N4 spacers (30, 35) on the sides of it.;

-A BPSG layer (37) is conformably deposited onto the surface of the gate stack, and the exposed surfaces of the Si wafer.;

-A patterned photo resist etch mask (40) is formed onto the surface of the BPSG layer (37).;

-The BPSG layer (37) is selectively dry etched relative to both the Si3N4 cap, Si3N4 spacers, and the source/drain regions (39) of the cz-Si wafer using a plasma comprised of (CH2F2-CF4). During this etch step, the newly exposed surface of the pad oxide (31) is also etched to expose the surface of the source/drain regions (39) of the cz-Si wafer.;

-The photo resist etch mask (40) is then removed from the surface of the wafer.;

-An Al alloy wiring layer (42) is then formed in the opening on either side of the gate electrode such that the Al wiring layer (42) contacts the source/drain (39) regions of the Si wafer.; and

-The Al wiring layer is then patterned using a dry etch process, and patterned photo resist etch mask.

This is discussed specifically in columns 6-11; and discussed in general in columns 1-14. This is shown specifically in figures 3A-3N; and shown in general in figures 1-5. Kasai fails, however, to specifically disclose the following aspects of applicant's claimed invention:

-the usage of the specific etch process parameters in the etch process taught above which are claimed by the applicant

It would have been prima facie obvious to employ any of a variety of different etch process parameters in the etch process taught above including those specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to employ the specific etch process parameters claimed by the applicant based upon In re Aller as cited as cited below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

Further, all of applicant's claimed process parameters are recognized results effective variables in the plasma etching arts whose selection would merely involve routine experimentation.

19. Claims 13-14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mele et. al. (5,037,777).

Mele et. al. disclose a process for forming a multi-layer semiconductor structure which is comprised of the following steps:

-A pair of gate stacks are formed parallel to each other on the surface of a cz-Si wafer (40). The gate stack is comprised of a SiO2 cap layer (44)/a conductive gate layer (42)/a pad oxide (46).;

-A layer of undoped SiO2 (48) is conformably deposited onto the surface of both gate stacks, and the exposed surface of the Si wafer (40).;

-A layer of BPSG (52) is conformably deposited onto the surface of the undoped SiO2 layer (48).;

-A patterned photo resist etch mask (54) is formed on the surface of the BPSG layer (52).;

-The BPSG layer (52) is selectively plasma etched to the underlying undoped SiO2 etch-stop layer (48) using a plasma comprised of (CF4-O2).;

-The undoped SiO2 layer (48) is then etched to form undoped sidewall spacers (56) on the sides of the pair of parallel gates. In this etch process, a portion of the cap SiO2 layer (44) on the top surface of the gate is also partially etched.;

-The photo resist etch mask (54) is then removed from the surface of the wafer.; and

-A conductive layer (59) is then conformably deposited onto the surface of the wafer to form a contact between the two parallel gate structure on the wafer surface. This conductive layer is then patterned using an etch process which employs a patterned photo resist etch mask.

This is discussed specifically in columns 4-5; and discussed in general in columns 1-10. This is shown specifically in figures 3-5; and shown in general in figures 1-5. Mele et. al. fail, however, to specifically disclose the following aspects of applicant's claimed invention:

-the usage of the specific etch process parameters in the etch process taught above to achieve the etch selectivity between the BPSG layer, and the SiO2 layers which is specifically claimed by the applicant

It would have been prima facie obvious to employ any of a variety of different etch process parameters to achieve any of a variety of different etch selectivities between the BPSG layer to be dry etched relative to the SiO2 layer which functions as an etch-stop in the etch process taught above including those specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to employ the specific etch process parameters claimed by the applicant to achieve the specific etch selectivities between the etched BPSG layer, and the SiO2 etch-stop based upon In re Aller as cited above.

Further, all of applicant's claimed process parameters are recognized results effective variables in the plasma etching arts whose selection would merely involve routine experimentation.

20. Claims 18-22, 24-29, 37-38, 40-44, 46, 50-52, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et. al. (5,677,227).

Yang et. al. disclose a process for making a self-aligned capacitor node contact which is comprised of the following steps:

-Multiple parallel gate structures are formed on the surface of a Si wafer, and on the surface of a field oxide layer (2) on the Si wafer (1). The gate structures are comprised of a laminated structure of Si3N4 cap layer (7)/ SiO2 cap layer (6)/ WSi2 layer (5)/ polysi layer (4)/ pad SiO2 (3).;

-A Si3N4 sidewall spacer (9) is formed on the sidewalls of the gate electrodes.;

-A BPSG layer is conformably deposited onto the surface of the wafer.;

-A patterned photo resist etch mask is formed on the surface of the BPSG layer.;

-The BPSG layer is selectively plasma etched relative to the field oxide layer (2), the source/drain region (10) in the Si wafer (1), the Si3N4 sidewall spacer (9), and the Si3N4 cap (7) in a plasma comprised of CHF3.;

-A polysi layer (13) is conformably deposited onto the surface of the wafer.;

-A WSi2 layer (14) is conformably deposited onto the surface of the wafer.;

-A SiO2 layer (15) is conformably deposited onto the surface of the wafer.;

-A Si3N4 layer (16) is conformably deposited onto the surface of the wafer.;

-A patterned photo resist etch mask (17) is formed onto the surface of the wafer.; and

-The Si3N4 (16)/SiO2 (15)/ WSi2 (14)/ polysi (13) layers are etched to form a gate stack which is aligned over the openings between adjacent gates in an underlying layer of circuitry. The bottom polysi layer (13) of this top level of gates forms a metal plug (i.e.-polysi) between the gates in the bottom level of gates.

This is discussed specifically in columns 2-5; and discussed in general in columns 1-12. This is shown specifically in figures 1-6; and shown in general in figures 1-17. Yang et. al. fail, however, to specifically disclose the following aspects of applicant's claimed invention:

-the usage of the specific etch process parameters in the etch process taught above to achieve the etch selectivity between the BPSG layer, and the SiO2 layers which is specifically claimed by the applicant; and

-the specific usage of the type of etching apparatus claimed by the applicant

It would have been prima facie obvious to employ any of a variety of different etch process parameters to achieve any of a variety of different etch selectivities between the BPSG layer to be dry etched relative to the SiO2 field oxide layer which functions as an etch-stop in the etch process taught above including those specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to employ the specific etch process parameters claimed by the applicant to achieve the specific etch selectivities between the etched BPSG layer, and the SiO2 etch-stop based upon In re Aller as cited above.

Further, all of applicant's claimed process parameters are recognized results effective variables in the plasma etching arts whose selection would merely involve routine experimentation.

It would have been obvious to one skilled in the art to employ any of a variety of different types of plasma etchers to conduct the plasma etching process taught above including those specific types of etching apparatus which are claimed by the applicant based upon the following. The usage of the specific types of plasma etchers which are claimed by the applicant for conducting their claimed plasma etching process simply involves the usage of an alternative, and at least equivalent means to those means specifically taught for conducting the etch process taught above. Further, the usage of the types of plasma etchers claimed by the applicant is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.)

Further, applicant did not invent the types of plasma etching apparatus which he is claiming to use to conduct his dry etching process. Applicant is simply using prior art etching apparatus whose usage in the plasma etching arts is well known to specifically conduct his claimed etching process.

21. Claims 1-10, and 12 are allowed.

22. Claims 11, and 30-36 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

23. Claims 23, and 39 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. Claims 45, and 53 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

25. Applicant's arguments with respect to claims of record have been considered but are moot in view of the new ground(s) of rejection.

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -308-3599.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.

George A. Goudreau/gag

Examiner AU 1763